98-0156

The invention relates to the computer engineering, microelectronics and can be used for the production and exploitation of supra-integrated circuits with incorporated compact means of testing and diagnostics.

The method for testing of operative memories with unipositional logical storage locations consists in the fact that the number of testing signals is chosen equal to the number of different stable states of one storage location, at the beginning of the testing cycle, the first and the second testing signals are registered correspondingly into the first two storage locations of the device with the capacitance m (m - the number of the storage locations), wherein the combination of tes-ting signals is selected unnull.

Then, it is repeated m - 2 times the next sequence of operations: it is read-out and summed according to the modulus two the content of the storage locations, wherein current testing signals are stored, afterwards the second testing signal is considered as the first testing signal and the result of summing according to the modulus two is considered as the second testing signal, it is registered the second testing signal into the next sto-rage location of the operative memory.

The resulting combination of testing signals is compared with the controlling one and if they coincide there are realized testing cycles with the other initial unnull combinations of the testing signals values to the first discrepancy of the resulting combination with the controlling one and it is determined the serviceability of the operative memory.

The technical result consists in detecting constant defects and defects of the storage locations mutual influence by introducing the “feedback“ and forming of the testing signals sequence by means of the memory.

Claims: 1